WHAT IS CLAIMED IS:

1. A method of manufacturing an integrated circuit, the method comprising:

providing a gate dielectric layer above a top surface of a substrate;

providing a silicon and nitrogen containing layer above the gate dielectric layer;

providing an oxide layer above the silicon and nitrogen containing layer;

selectively etching the oxide layer to form a first trench in the oxide layer;

selectively etching the silicon and nitrogen containing layer to form a second trench in the silicon and nitrogen containing layer, the second trench being narrower than the first trench and being disposed below the first trench; and

providing a gate conductor material in the first trench and the second trench.

2. The method of claim 1, further comprising removing the oxide layer.

3. The method of claim 2, further comprising:

removing portions of the silicon and nitrogen containing layer, whereby a pair of spacers remain underneath the gate conductor material in the first trench.

4. The method of claim 3, wherein the gate conductor material is removed by a polishing process.

5. The method of claim 3, wherein the silicon and nitrogen containing layer includes silicon rich nitride.

6. The method of claim 1, wherein the selective etching the silicon and nitrogen containing layer includes a RELACS process.

7. The method of claim 1, wherein the silicon and nitrogen containing layer includes SiON or silicon rich nitride.

8. The method of claim 7, wherein the silicon and nitrogen containing layer is a silicon rich nitride layer.

9. The method of claim 1, wherein a width of the first trench is at least 250 Å and less than 1600 Å.

10. The method of claim 9, wherein the width of the second trench is at least 400 Å and less than 2100 Å.

11. A method of manufacturing an ultra-large scale integrated circuit including a transistor with a T-shaped gate conductor, the method includes steps of:

providing a first layer above a substrate, the first layer being a silicon rich nitride layer or a silicon oxynitride layer;

providing an oxide layer over the first layer;

forming a first trench in the oxide layer;

forming a second trench in the first layer, the second trench having a smaller width than the first trench; and

providing a gate conductor material in the first trench and in the second trench to form the T-shaped gate conductor.

12. The method of claim 11, further comprising removing the oxide layer.

13. The method of claim 12, further comprising removing portions of the first layer to leave spacers underneath the gate conductor material in the first trench, the removal process utilizing the gate conductor material as a mask.

14. The method of claim 13, wherein the first layer is silicon rich nitride.

15. A method of manufacturing a gate conductor for an integrated circuit, the method comprising:

providing a first layer above a gate dielectric layer, the gate dielectric layer being above a substrate, the first layer including silicon oxynitride or silicon rich nitride;

forming an aperture in the first layer utilizing a RELACS process;

filling the aperture with a gate conductor material; and

removing the gate conductor material above the first layer.

16. The method of claim 15, further comprising:

providing an oxide layer above the first layer and forming an aperture in the oxide layer before forming the aperture in the first layer.

17. The method of claim 16, wherein the gate conductor material is doped or undoped polysilicon material.

18. The method of claim 17, wherein a T-shaped gate conductor is formed.

19. The method of claim 16, wherein the gate conductor material is also provided in the aperture in the oxide layer.

20. The method of claim 16, wherein the oxide layer is silicon dioxide.